ANALOG DEVICES
PRECISION MONOLITHICS

Quad 12–Bit Serial Voltage–Output DAC

PRELIMINARY

DAC-8420

FEATURES

Guaranteed Monotonic Over Temperature
Unipolar Or Bipolar Operation
Buffered Voltage Outputs
High–Speed Serial Digital Interface
Reset to Zero– Or Center–Scale
Wide Supply Range, +5V–Only to ±15V
Low Power Consumption (60mW max)
Available in 16-pin DIP and SO Packages

APPLICATIONS

Software-Controlled Calibration
Servo Controls
Process Control and Automation

GENERAL DESCRIPTION

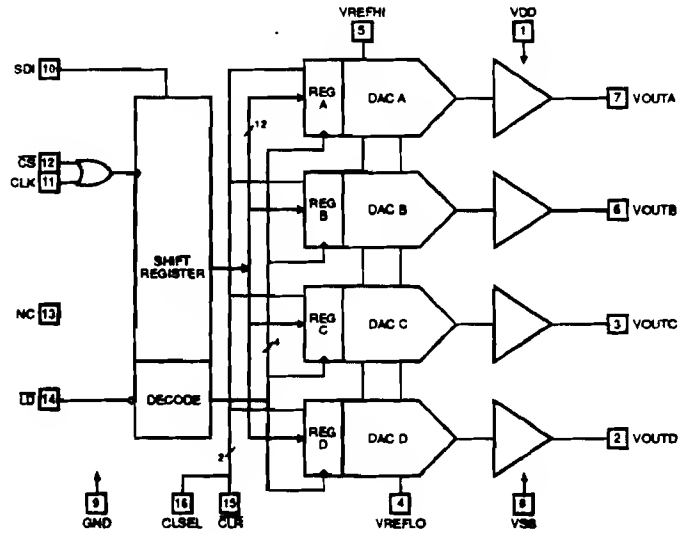
The DAC-8420 is a quad, 12-bit voltage-output DAC with serial digital interface, in a 16-pin package. Utilizing BiCMOS technology, this monolithic device features unusually high circuit density and low power consumption. The simple, east-to-use serial digital input and fully buffered analog voltage outputs require no external components to achieve specified performance.

The three-wire serial digital input is easily interfaced to microprocessors running up to 20MHz clock rates, with minimal additional circuitry. Each DAC is addressed individually by a 16-bit serial word consisting of a 12-bit data word with an address header. The user-programmable reset control CLR forces all four DAC outputs to either zero- or midscale, asynchronously overriding the current DAC register values. The output voltage range, determined by the inputs VREFHI and VREFLO, is set by the user for positive or negative Unipolar or Bipolar signal swings within the supplies. This structure allows considerable design flexibility, yielding circuits with low temperature drift.

The DAC-8420 is available in 16-pin epoxy DIP, CerDIP, and wide- body SO (small-outline surface mount) packages. Operation is specified with supplies ranging from +5V-only to ±15V, with references of +2.5V to ±10V respectively. Power dissipation when operation from ±15V supplies is less than 330mW(max), and only 60mW(max) with a +5V supply.

For applications requiring product meeting MIL-STD-883, contact your local sales office for he DAC-8420/883 data sheet, which specifies operation over the -55°C to +125°C temperature range.

FUNCTIONAL DIAGRAM



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DAC-8420– SPECIFICATIONS

ELECTRICAL CHARACTERISTICS at V_{DD}=+5.0V ±5%, V_{SS}=0.0V, V_{REFH}=+2.5V, V_{REFL}=0.0V, and V_{SS} = -5.0V±5%, V_{REFL}=-2.5V. -40°C ≤ T_A ≤ +85°C unless otherwise specified. See Note 1 for supply variations.

PARAMETER		COND	MIN	TYP	MAX	UNITS
Integral Linearity "E"	INL			.5	±1	LSB
Integral Linearity "E"	INL	Note 2, V_{SS} = 0V			±2	LSB
Integral Linearity "F"	INL				±2	LSB
Integral Linearity "F"	INL	Note 2, V_{SS} = 0V			±4	LSB
Differential Linearity	DNL	Monotonic over temp.	-1			LSB
Min Scale Error	ZSE				±4	LSB
Full Scale Error	FSE				±4	LSB
Min Scale Error	ZSE	Note 2, V_{SS} = 0V			±8	LSB
Full Scale Error	FSE	Note 2, V_{SS} = 0V			±8	LSB
Min Scale Tempco				100		ppm/°C
Full Scale Tempco				100		ppm/°C
MATCHING PERFORMANCE						
Linearity Matching				±1		LSB
REFERENCE						
Positive Reference Input Range		Note 2	V_{REFL}+2.5		V_{DD}-2.5	V
Negative Reference Input Range		Note 2	V_{SS}		V_{REFH}-2.5	V
Negative Reference Input Range		Note 2, V_{SS} = 0V	0		V_{REFH}-2.5	V
Reference High Input Current	I_{REFH}	Code 000_H	0		+1.0	mA
AMPLIFIER CHARACTERISTICS						
Output Current	I_{OUT}		-1.25		+1.25	mA
Settling Time	t_s	to .01%		6		µsec
Slew Rate	SR	10% to 90%		2.2		V/µsec
LOGIC CHARACTERISTICS						
Logic Input High Voltage	V_{INH}	T_A = +25°C	2.4			V
Logic Input Low Voltage	V_{INL}	T_A = +25°C			0.8	V
Logic Input Current	I_{IN}				1	µA
Input Capacitance	C_{IN}			8		pF
LOGIC TIMING CHARACTERISTICS (Note 3)						
Data Setup Time	tds					ns
Data Hold	tdh					ns
Clock Pulse Width HIGH	tch		60			ns
Clock Pulse Width LOW	tcl		60			ns
Select Time	tcss					ns
Deselect Delay	tcsh					ns
Load Disable Time	tld1					ns
Load Delay	tld2					ns
Load Pulse Width	tldw					ns
Clear Pulse Width	tclrw					ns
Settling Time	ts					ns
SUPPLY CHARACTERISTICS						
Power Supply Sensitivity	PSS			100		ppm/V
Positive Supply Current	I_{DD}			7	12	mA
Negative Supply Current	I_{SS}		-10	-7		mA
Power Dissipation	P_{DISS}				60	mW

NOTES:

1. All supplies can be varied ±5% and operation is guaranteed. Device is tested with V_{DD}=+4.75V.
2. Operation is guaranteed over this reference range, but linearity is neither tested nor guaranteed.
3. All input control signals are specified with tr = tf = 5ns (10% to 90% of +5V) and timed from a voltage level of 1.6V.

DAC-8420 – ±15 Volt Specifications

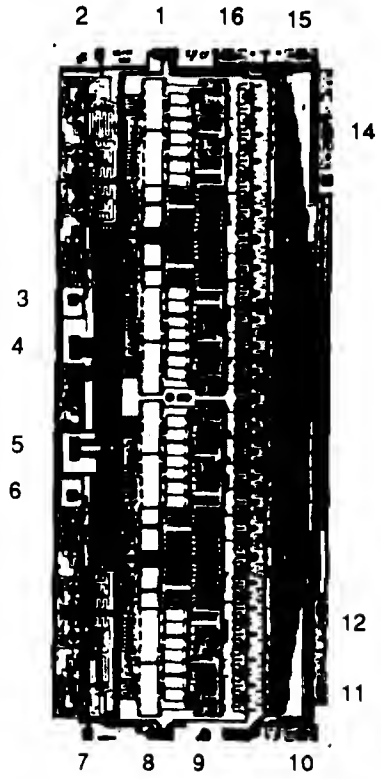
ELECTRICAL CHARACTERISTICS at V_{DD}=+15.0V, V_{SS}=-15.0V, V_{REFH}=+10.0V, V_{REFL}=-10.0V, -40°C ≤ T_A ≤ +85°C unless otherwise specified. See Note 1 for supply variations.

PARAMETER		COND	MIN	TYP	MAX	UNITS
Integral Linearity "E"	INL			.25	±.5	LSB
Integral Linearity "F"	INL				±1	LSB
Differential Linearity	DNL	Monotonic Over Temperature	-1			LSB
Min Scale Error	ZSE	R_L = 2kΩ			±2	LSB
Full Scale Error	FSE	R_L = 2kΩ			±2	LSB
Min Scale Tempco	TCZSE	R_L = 2kΩ		15		ppm/°C
Full Scale Tempco	TCFSE	R_L = 2kΩ		20		ppm/°C
MATCHING PERFORMANCE						
Linearity Matching				±1		LSB
REFERENCE						
Positive Reference Input Range		Note 2	V_{REFL}+2.5		V_{DD}-2.5	V
Negative Reference Input Range		Note 2	-10		V_{REFH}-2.5	V
Reference High Input Current	I_{REFH}		-2.75	+1.5	+2.75	mA
Reference Low Input Current	I_{REFL}		-2.75	-2	0	mA
AMPLIFIER CHARACTERISTICS						
Output Current	I_{OUT}		-5		+5	mA
Settling Time	t_s	to .01%		8		µsec
Slew Rate	SR	10% to 90%		2.3		V/µsec
LOGIC CHARACTERISTICS						
Logic Input High Voltage	V_{INH}	T_A = +25°C	2.4			V
Logic Input Low Voltage	V_{INL}	T_A = +25°C			0.8	V
Logic Input Current	I_{IN}				1	µA
Input Capacitance	C_{IN}			8		pF
Crosstalk				>72		dB
Large Signal Bandwidth		-3dB, V_{REFH} = 1 to +10V typ		160		kHz
LOGIC TIMING CHARACTERISTICS (Note 3)						
Data Setup Time	tds		20			ns
Data Hold	tdh		20			ns
Clock Pulse Width HIGH	tch		30			ns
Clock Pulse Width LOW	tcl		50			ns
Select Time	tcss		50			ns
Deselect Delay	tcsh		10			ns
Load Disable Time	tld1		50			ns
Load Delay	tld2		10			ns
Load Pulse Width	tldw		40			ns
Clear Pulse Width	tclrw		50			ns
Settling Time	ts			6		µs
SUPPLY CHARACTERISTICS						
Power Supply Sensitivity	PSS				150	ppm/V
Positive Supply Current	I_{DD}	VREFHI = +2.5V, VREFLO=-2.5V		7	12	mA
Negative Supply Current	I_{SS}		-10	-7		mA
Power Dissipation	P_{DISS}				330	mW

NOTES:

1. All supplies can be varied ±5% and operation is guaranteed. Device is tested with nominal supplies.
2. Operation is guaranteed over this reference range, but linearity is neither tested nor guaranteed.
3. All input control signals are specified with tr = tf = 5ns (10% to 90% of +5V) and timed from a voltage level of 1.6V.

DICE CHARACTERISTICS



1. VDD(Substrate)
2. VOUTD
3. VOUTC
4. VREFLO
5. VREFHI
6. VOUTB
7. VOUTA
8. VSS
9. GND
10. SDI
11. CLK
12. CS\
13. NC
14. LD\
15. CLR\
16. CLSEL

DIE SIZE 0.119 X 0.283 inch, 33,677sq. mils
(3.023 X 7.188 mm, 21.73 sq. mm)

For additional DICE ordering information, refer to Data Book.

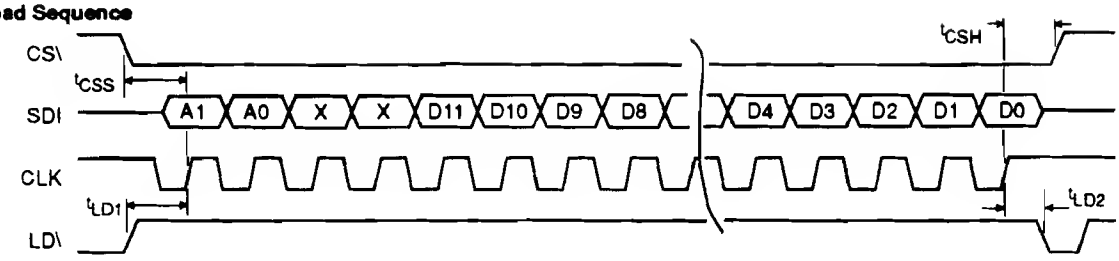
WAFER TEST LIMITS at V_{DD} = +15.0 V , V_{SS} =-15.0 V, VREFHI = +10.0V, VREFLO = -10.0V, T_A = +25°C, unless otherwise specified.

			DAC-8420G	
PARAMETER	**SYMBOL**	**CONDITIONS**	**LIMIT**	**UNITS**
Integral Nonlinearity	INL		±1	LSB MAX
Differential Nonlinearity	DNL		±1	LSB MAX
Min Scale Offset			±1	LSB MAX
Max Scale Offset			±1	LSB MAX
Logic Input High Voltage	V_{INH}		2.4	V MIN
Logic Input Low Voltage	V_{INL}		0.8	V MAX
Logic Input Current	I_{IN}		1	µA MAX
Positive Supply Current	I_{DD}		15	mA MAX
Negative Supply Current	I_{SS}		10	mA MAX

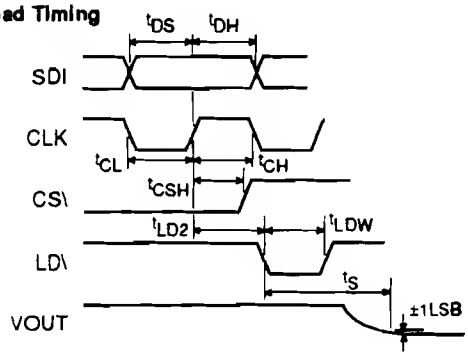
NOTE:
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TIMING DIAGRAM

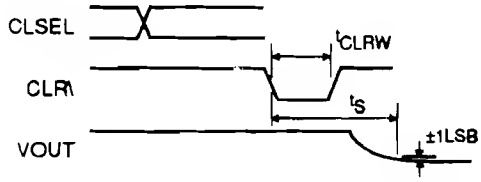
Data Load Sequence



Data Load Timing



Clear Timing



ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

V_{SS} to V_{DD}	-0.3 V, +36.0 V
V_{SS} to GND	-0.3 V, +18.0V
V_{DD} to GND	+0.3 V, -18.0 V
V_{SS} to VREFLO	-0.3 V, V_{SS} - 2.0V
VREFHI to VREFLO	+2.0 V, V_{SS} - V_{DD}
VREFHI TO V_{DD}	+2.0 V, +33.0V
IREFHI, IREFLO	? mA
Current into Any Pin	± 15 mA
Digital Input Voltage to DGND	-0.3V, V_{LOGIC} +0.3V
Operating Temperature Range	
EP, FP, ES, FS, ET, FT	-40°C to +85°C
BT	-55°C to +125°C
Dice Junction Temperature	+150°C
Storage Temperature	-65°C to +150°C
Power Dissipation	1000mW
Lead Temperature (Soldering, 60 sec.)	300°C

	Thermal Resistance	
PACKAGE TYPE	Θ_{JA}[1] UNITS	Θ_{JC}
16-Pin Plastic DIP (P)	xx °C/W	xx
16-Pin Hermetic DIP (T)	xx °C/W	xx
16-Lead Small Outline Surface Mount (S)	xx °C/W	xx

NOTE:

1. Θ_{jA} is specified for worst case mounting conditions, i.e., Θ_{jA} is specified for device in socket.

1. Stressesabove those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to the above maximum rating conditions for extended periods may affect device reliability.
2. Digital inputs and outputs are protected, however, permanent damage r occur on unprotected units from high-energy electrostatic fields. Keep unit conductive foam or packaging at all times until ready to use. Use proper anti-static handling procedures.
3. Remove power before inserting or removing units from their sockets.
4. Analog Outputs are protected from short circuits to ground or either supply.

CAUTION:

PIN FUNCTION DESCRIPTION

POWER SUPPLIES
VDD: Positive Supply, +5V to +15V.
VSS: Negative Supply, 0 to -15V.
GND: Digital Ground.

CLOCK
CLK: System Serial Data Clock Input, TTL/CMOS levels. Data presented to the input SDI on the falling edge of clock is shifted into the internal serial-parallel input register. This input is logically ANDed with CS\.

CONTROL INPUTS (All are CMOS/TTL compatible)
CLR\: Asynchronous Clear, active low. Sets internal data registers A - D to zero or mid-scale, depending on current state of CLSEL. The data in the serial input shift register is unaffected by this control.
CLSEL: Determines action of CLR\. If HIGH, a Clear command will set the internal DAC registers A - D to mid-scale (800_H). If LOW, the registers are set to zero (000_H).
CS\: Device Chip Select, active low. This input is logically ANDed with the clock and disables the serial data register input when HIGH. When LOW, data input clocking is enabled. See the Control Function Table.
LD\: Asynchronous DAC Register Load Control, active low. The data currently contained in the serial input shift register is shifted out to the DAC data registers on the falling edge of LD\, independent of CS\. Input data must remain stable while LD\ is LOW.
DATA INPUT (All are CMOS/TTL compatible)
SDI: Serial Data Input. Data presented to this pin is loaded into the internal serial-parallel shift register, which shifts data in beginning with DAC address bit A1. This input is ignored when CS\ is HIGH.
The format of the 16-bit serial word is:

(FIRST)															(LAST)
B0	B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11	B12	B13	B14	B15
A1	A0	NC	NC	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
- Address Word -				(MSB)				- - - DAC Data Word - - -							(LSB)

REFERENCE INPUTS
VREFHI: Upper DAC ladder reference voltage input. Allowable range is (VDD-2.5V) to (VREFLO+2.5V).
VREFLO: Lower DAC ladder reference voltage input, equal to zero scale output. Allowable range is VSS to (VREFHI-2.5V).

ANALOG OUTPUTS
VOUTA through VOUTD: Four buffered DAC voltage outputs.

CONTROL FUNCTION TABLE

CLK[1]	CS\[1]	LD\	CLR\	CLSEL	Serial Input Shift Register	DAC Registers A– D
NC	H	H	L	H	No Change	Loads midscale value (40_H)
NC	H	H	L	L	No Change	Loads zero scale value (00_H)
NC	H	H	↑	H/L	No Change	Latches value
↓	L	H	H	NC	Reads in serial input SDI	No Change
↑	L	H	H	NC	Shifts register one bit.	No Change
H	NC (↑)	↓	H	NC	No Change	Loads the serial data word [2]
H	NC	L	H	NC	No Change	Transparent[3]
NC	H	H	H	NC	No Change	No Change

NC = Don't Care.

Notes
1. CS\ and CLK are interchangeable.
2. Returning CS\ HIGH while CLK is HIGH avoids an additional "false clock" of serial input data. See Note 1.
3. Do not clock in serial data while LD\ is LOW.

DIGITAL INTERFACE OPERATION

The serial input of the DAC-8420, consisting of CS\, SDI, and LD\, is easily interfaced to a wide variety of microprocessor serial ports. As shown in the Control Function Table and the Timing Diagram, while CS\ is LOW the data presented to the input SDI is shifted into the internal serial/parallel shift register on the rising edge of the clock, with the address MSB first, data LSB last, The data format, shown above, is two bits of DAC address and two "don't care" fill bits, followed by the 12-bit DAC data word. Once all 16 bits of the serial data word have been input, the load control LD\ is strobed and the word is parallel-shifted out onto the internal data bus. The two address bits are decoded and used to route the 12-bit data word to the appropriate DAC data register.

DAC ADDRESS WORD DECODE TABLE

A1	A0	DAC Addressed
0	0	DAC A
0	1	DAC B
1	0	DAC C
1	1	DAC D

ANALOG OUTPUT CODE TABLE

DAC Data Word (HEX)	VOUT	Note
FFF	$VREFLO + \frac{(VREFHI - VREFLO)}{4096} \times 4095$	Full-scale output
801	$VREFLO + \frac{(VREFHI - VREFLO)}{4096} \times 2049$	Midscale + 1
800	$VREFLO + \frac{(VREFHI - VREFLO)}{4096} \times 2048$	Midscale
7FF	$VREFLO + \frac{(VREFHI - VREFLO)}{4096} \times 2047$	Midscale - 1
000	$VREFLO + \frac{(VREFHI - VREFLO)}{4096} \times 0$	Zero-scale

PROGRAMMING THE ANALOG OUTPUTS

The unique differential reference structure of the DAC-8420 allows the user to tailor the output voltage range precisely to the needs of the application. Instead of wasting DAC resolution on an unused region near the positive or negative rail, the DAC-8420 allows the user to determine both the upper and lower limits of the analog output voltage range. Thus, as shown in the Analog Output Code Table the outputs of DACs A through D range between VREFHI and VREFLO, within the limits specified in the Electrical Characteristics tables.

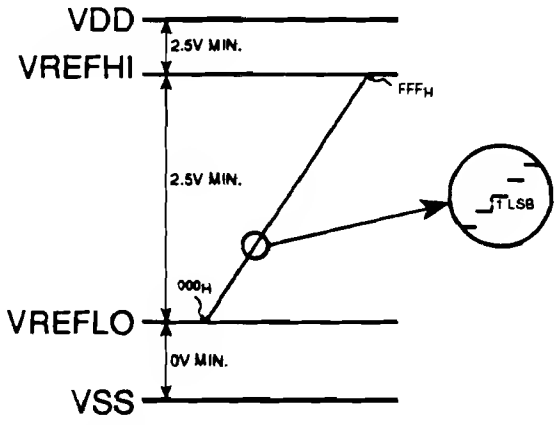
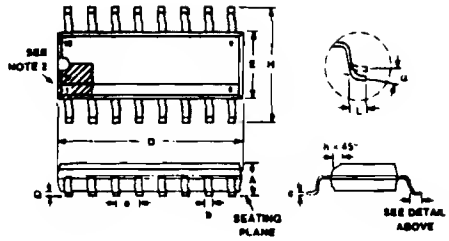


Figure X. Output Voltage Range Programming

PACKAGE DIMENSIONS

16-Pin Epoxy DIP (P)

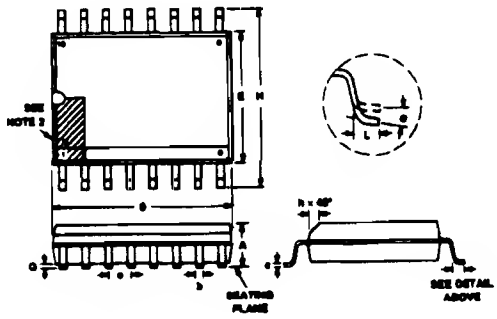


SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	
b	0.0138	0.0192	0.35	0.49	
c	0.0075	0.0098	0.19	0.25	
D	0.3859	0.3937	9.80	10.00	
E	0.1497	0.1574	3.80	4.00	
H	0.2284	0.2440	5.80	6.20	
e	0.0500 BSC		1.27 BSC		
h	0.0099	0.0196	0.25	0.50	
L	0.0160	0.0500	0.41	1.27	
Q	0.0040	0.0098	0.10	0.25	
α	0°	8°	0°	8°	

NOTES

1. Package dimensions conform to JEDEC specification MS-012-AC (Issue A, June 1985).
2. Index area; a dimple or lead one identification mark is located adjacent to lead one and is within the shaded area shown.

16-Pin SOIC (S)



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0926	0.1043	2.35	2.65	
b	0.0138	0.0192	0.35	0.49	
c	0.0091	0.0125	0.23	0.32	
D	0.3977	0.4133	10.10	10.50	
E	0.2914	0.2992	7.40	7.60	
H	0.3977	0.4193	10.10	10.50	
e	0.0500 BSC		1.27 BSC		
h	0.0098	0.0291	0.25	0.74	
L	0.0157	0.0500	0.40	1.27	
Q	0.0040	0.0118	0.10	0.30	
α	0°	8°	0°	8°	

NOTES

1. Package dimensions conform to JEDEC specification MS-013-AA (Issue A, June 1985).
2. Index area; a dimple or lead one identification mark is located adjacent to lead one and is within the shaded area shown.